WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a semiconductor substrate of a first conductivity type;

a semiconductor layer of a second conductivity type provided on said semiconductor substrate;

a first impurity region of said first conductivity type provided in said semiconductor layer, extending from an upper surface of said semiconductor layer to reach an interface with said semiconductor substrate, said first impurity region defining a RESURF isolation region;

a first trench isolation structure provided in said semiconductor layer defined in said RESURF isolation region to be connected to said first impurity region, extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said first trench isolation structure and said first impurity region together defining a first trench isolation region in said RESURF isolation region;

a semiconductor element provided in said semiconductor layer defined in said RESURF isolation region excluding said first trench isolation region; and

a first MOS transistor, comprising

a second impurity region of said second conductivity type provided in said upper surface of said semiconductor layer defined in said first trench isolation region, said second impurity region being connected to a drain electrode of said first MOS transistor,

a third impurity region of said first conductivity type provided in said upper surface of said semiconductor layer defined between said first and second impurity regions, and

a first source region of said second conductivity type provided in an upper surface of said third impurity region,

wherein said semiconductor device further comprises a buried impurity region of said second conductivity type provided under said second impurity region and at said interface between said semiconductor layer and said semiconductor substrate, said buried impurity region being higher in impurity concentration than said semiconductor layer.

2. The semiconductor device according to claim 1, further comprising

a second trench isolation structure separated by a certain distance from said first trench isolation structure, said second trench isolation structure being provided in said semiconductor layer defined in said RESURF isolation region to be connected to said first impurity region, extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said second trench isolation structure, said first impurity region, and said first trench isolation structure together defining said first trench isolation region in said RESURF isolation region.

3. The semiconductor device according to claim 1,

wherein said first trench isolation structure comprises an in-line portion which extends from said first impurity region towards said second impurity region, said in-line portion including

a plurality of spaced-apart conductive films provided in said semiconductor layer defined in said RESURF isolation region, aligning in the extending direction of said in-line portion, and

a plurality of first insulating films for covering respective ones of said plurality of conductive films, at surfaces buried in said semiconductor layer.

4. The semiconductor device according to claim 3,

wherein openings between adjacent ones of said plurality of conductive films are filled with said plurality of first insulating films.

5. The semiconductor device according to claim 2,

wherein said first and second trench isolation structures each comprise an in-line portion which extends from said first impurity region towards said second impurity region, said in-line portion including

a plurality of spaced-apart conductive films provided in said semiconductor layer defined in said RESURF isolation region, aligning in the extending direction of said in-line portion, and

a plurality of insulating films for covering respective ones of said plurality of conductive films, at surfaces buried in said semiconductor layer.

6. The semiconductor device according to claim 1,

wherein said first trench isolation structure reaches said semiconductor substrate, and

wherein an end portion of said first trench isolation structure reaches a depth shallower than the greatest possible depth of said buried impurity region.

7. The semiconductor device according to claim 1,

wherein said first trench isolation structure comprises an in-line portion which extends from said first impurity region towards said second impurity region, said in-line portion including

a plurality of spaced-apart conductive films provided in said semiconductor layer defined in said RESURF isolation region, aligning in the extending direction of said in-line portion, and

a plurality of spaced-apart insulating films for covering respective ones of said plurality of conductive films, at surfaces buried in said semiconductor layer, and

wherein said semiconductor device further comprises a fourth impurity region provided in said upper surface of said semiconductor layer defined in said RESURF isolation region, surrounding each one of said plurality of insulating films while filling openings between adjacent ones of said plurality of insulating films.

8. The semiconductor device according to claim 7,

wherein said fourth impurity region is depleted in its entirety when a PN junction between said fourth impurity region and said semiconductor layer is subjected to application of a reverse voltage.

9. The semiconductor device according to claim 1, further comprising

a second trench isolation structure provided in said semiconductor layer defined in said RESURF isolation region to be connected to said first impurity region, extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said second trench isolation structure and said first impurity region together defining a second trench isolation region in said RESURF isolation region, and

a second MOS transistor, comprising

a fourth impurity region of said second conductivity type provided in said upper surface of said semiconductor layer defined in said second trench isolation region, said

fourth impurity region being connected to a drain electrode of said second MOS transistor,

a fifth impurity region of said first conductivity type provided in said upper surface of said semiconductor layer defined between said first and fourth impurity regions, and

a second source region of said second conductivity type provided in an upper surface of said fifth impurity region.

10. The semiconductor device according to claim 1, comprising

an interconnect line provided over said first trench isolation structure to be electrically connected to said drain electrode, and

a field plate held between said first trench isolation structure and said interconnect line,

wherein said field plate is a floating electrode, an electrode which is electrically connected to said semiconductor layer defined in said first trench isolation region, or an electrode which is electrically connected to said semiconductor layer defined in said RESURF isolation region excluding said first trench isolation region.

11. The semiconductor device according to claim 3, further comprising

a second insulating film provided on said semiconductor layer defined between said first impurity region and said buried impurity region, and

a plurality of field plates provided on said second insulating film,

wherein said plurality of conductive films are exposed from said upper surface of said semiconductor layer, and

wherein said plurality of field plates are respectively connected to said plurality

of conductive films.

12. A method of manufacturing a semiconductor device, said semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a semiconductor layer of a second conductivity type provided on said semiconductor substrate;

a first impurity region of said first conductivity type provided in said semiconductor layer, extending from an upper surface of said semiconductor layer to reach an interface with said semiconductor substrate, said first impurity region defining a RESURF isolation region;

a trench isolation structure provided in said semiconductor layer defined in said RESURF isolation region to be connected to said first impurity region, extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said trench isolation structure and said first impurity region together defining a trench isolation region in said RESURF isolation region;

a semiconductor element provided in said semiconductor layer defined in said RESURF isolation region excluding said trench isolation region;

a MOS transistor, comprising

a second impurity region of said second conductivity type provided in said upper surface of said semiconductor layer defined in said trench isolation region, said second impurity region being connected to a drain electrode of said MOS transistor,

a third impurity region of said first conductivity type provided in said upper surface of said semiconductor layer defined between said first and second impurity

regions, and

a source region of said second conductivity type provided in an upper surface of said third impurity region; and

a buried impurity region of said second conductivity type provided under said second impurity region and at said interface between said semiconductor layer and said semiconductor substrate, said buried impurity region being higher in impurity concentration than said semiconductor layer,

wherein said trench isolation structure comprises an in-line portion which extends from said first impurity region towards said second impurity region, said in-line portion including

a plurality of spaced-apart conductive films provided in said semiconductor layer defined in said RESURF isolation region, aligning in the extending direction of said in-line portion, and

a plurality of insulating films for covering respective ones of said plurality of conductive films, at surfaces buried in said semiconductor layer,

said method comprising the steps of:

(a) providing said semiconductor layer on said semiconductor substrate;

(b) forming a plurality of trenches in said semiconductor layer to be separated by a certain distance, said plurality of trenches extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate;

(c) oxidizing respective inner walls of said plurality of trenches to provide said plurality of insulating films on respective inner surfaces of said plurality of trenches; and

(d) providing said plurality of conductive films to respectively fill said plurality of trenches,

wherein in said step (a), a distance between adjacent ones of said plurality of trenches is not more than a thickness of said plurality of insulating films.

13. A method of manufacturing a semiconductor device, said semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a semiconductor layer of a second conductivity type provided on said semiconductor substrate;

a first impurity region of said first conductivity type provided in said semiconductor layer, extending from an upper surface of said semiconductor layer to reach an interface with said semiconductor substrate, said first impurity region defining a RESURF isolation region;

a trench isolation structure provided in said semiconductor layer defined in said RESURF isolation region to be connected to said first impurity region, extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said trench isolation structure and said first impurity region together defining a trench isolation region in said RESURF isolation region;

a semiconductor element provided in said semiconductor layer defined in said RESURF isolation region excluding said trench isolation region;

a MOS transistor, comprising

a second impurity region of said second conductivity type provided in said upper surface of said semiconductor layer defined in said trench isolation region, said second impurity region being connected to a drain electrode of said MOS transistor,

a third impurity region of said first conductivity type provided in said upper

surface of said semiconductor layer defined between said first and second impurity regions, and

a source region of said second conductivity type provided in an upper surface of said third impurity region; and

a buried impurity region of said second conductivity type provided under said second impurity region and at said interface between said semiconductor layer and said semiconductor substrate, said buried impurity region being higher in impurity concentration than said semiconductor layer,

wherein said trench isolation structure comprises an in-line portion which extends from said first impurity region towards said second impurity region, said in-line portion including

a plurality of spaced-apart conductive films provided in said semiconductor layer defined in said RESURF isolation region, aligning in the extending direction of said in-line portion, and

a plurality of spaced-apart insulating films for covering respective ones of said plurality of conductive films, at surfaces buried in said semiconductor layer, and

wherein said semiconductor device further comprises a fourth impurity region provided in said upper surface of said semiconductor layer defined in said RESURF isolation region, surrounding each one of said plurality of insulating films while filling openings between adjacent ones of said plurality of insulating films,

said method comprising the steps of:

(a) providing said semiconductor layer on said semiconductor substrate;

(b) forming a plurality of trenches in said semiconductor layer to be separated by a certain distance, said plurality of trenches extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor

substrate;

(c) introducing impurities of said first conductivity type into respective inner walls of said plurality of trenches to provide said fourth impurity region;

(d) providing said plurality of insulating films on respective inner surfaces of said plurality of trenches; and

(e) providing said plurality of conductive films to respectively fill said plurality of trenches.

14. A method of manufacturing a semiconductor device, said semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a semiconductor layer of a second conductivity type provided on said semiconductor substrate;

a first impurity region of said first conductivity type provided in said semiconductor layer, extending from an upper surface of said semiconductor layer to reach an interface with said semiconductor substrate, said first impurity region defining a RESURF isolation region;

a trench isolation structure provided in said semiconductor layer defined in said RESURF isolation region to be connected to said first impurity region, extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said trench isolation structure and said first impurity region together defining a trench isolation region in said RESURF isolation region;

a semiconductor element provided in said semiconductor layer defined in said RESURF isolation region excluding said trench isolation region;

a MOS transistor, comprising

a second impurity region of said second conductivity type provided in said upper surface of said semiconductor layer defined in said trench isolation region, said second impurity region being connected to a drain electrode of said MOS transistor,

a third impurity region of said first conductivity type provided in said upper surface of said semiconductor layer defined between said first and second impurity regions, and

a source region of said second conductivity type provided in an upper surface of said third impurity region; and

a buried impurity region of said second conductivity type provided under said second impurity region and at said interface between said semiconductor layer and said semiconductor substrate, said buried impurity region being higher in impurity concentration than said semiconductor layer,

wherein said trench isolation structure comprises an in-line portion which extends from said first impurity region towards said second impurity region, said in-line portion including

a plurality of spaced-apart conductive films provided in said semiconductor layer defined in said RESURF isolation region, aligning in the extending direction of said in-line portion, and

a plurality of first insulating films for covering respective ones of said plurality of conductive films, at surfaces buried in said semiconductor layer,

wherein said semiconductor device further comprises

a second insulating film provided on said semiconductor layer defined between said first impurity region and said buried impurity region, and

a plurality of field plates provided on said second insulating film,

wherein said plurality of conductive films are exposed from said upper surface of said semiconductor layer, and

wherein said plurality of field plates are respectively connected to said plurality of conductive films,

said method comprising the steps of:

(a) providing said semiconductor layer on said semiconductor substrate;

(b) forming a plurality of trenches in said semiconductor layer to be separated by a certain distance, said plurality of trenches extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate;

(c) providing said plurality of first insulating films on respective inner surfaces of said plurality of trenches;

(d) providing said second insulating film on said semiconductor layer;

(e) depositing a conductive material on said second insulating film to fill said plurality of trenches; and

(f) patterning said conductive material to concurrently provide said plurality of conductive films and said plurality of field plates.

15. A method of evaluating manufacturing process of a semiconductor device, said semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a semiconductor layer of a second conductivity type provided on said semiconductor substrate;

a first impurity region of said first conductivity type provided in said semiconductor layer, extending from an upper surface of said semiconductor layer to

reach an interface with said semiconductor substrate, said first impurity region defining a RESURF isolation region;

a first trench isolation structure provided in said semiconductor layer defined in said RESURF isolation region to be connected to said first impurity region, extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said first trench isolation structure and said first impurity region together defining a trench isolation region in said RESURF isolation region;

a semiconductor element provided in said semiconductor layer defined in said RESURF isolation region excluding said trench isolation region;

a MOS transistor, comprising

a second impurity region of said second conductivity type provided in said upper surface of said semiconductor layer defined in said trench isolation region, said second impurity region being connected to a drain electrode of said MOS transistor,

a third impurity region of said first conductivity type provided in said upper surface of said semiconductor layer defined between said first and second impurity regions, and

a source region of said second conductivity type provided in an upper surface of said third impurity region; and

a buried impurity region of said second conductivity type provided under said second impurity region and at said interface between said semiconductor layer and said semiconductor substrate, said buried impurity region being higher in impurity concentration than said semiconductor layer,

wherein said first trench isolation structure comprises an in-line portion which extends from said first impurity region towards said second impurity region, said in-line

portion including

a plurality of spaced-apart first conductive films provided in said semiconductor layer defined in said RESURF isolation region, aligning in the extending direction of said in-line portion, and

a plurality of first insulating films for covering respective ones of said plurality of conductive films, at surfaces buried in said semiconductor layer,

wherein said semiconductor device comprises a plurality of test structures operative to function as a monitor to evaluate manufacturing process of said in-line portion of said first trench isolation structure, said plurality of test structures each comprising a second trench isolation structure for defining a certain region in said semiconductor layer, extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said second trench isolation structure including

a plurality of spaced-apart second conductive films provided in said semiconductor layer, and

a plurality of spaced-apart second insulating films for covering respective ones of said plurality of second conductive films, at surfaces buried in said semiconductor layer, and

wherein a distance between adjacent ones of said plurality of second insulating films differs between said plurality of test structures,

said method comprising the steps of:

(a) in each one of said plurality of test structures, measuring a leakage current flowing between said semiconductor layer opposite to said certain region with respect to said second trench isolation structure and said semiconductor layer in said certain region; and

(b) evaluating manufacturing process of said in-line portion in said first trench isolation structure using said leakage current measured in said step (a).